

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

Application No : 09/992,387 Confirmation No: 7595  
Applicants : Anthony L. Coyle et al.  
Filed : November 16, 2001  
TC/A.U. : 2822  
Examiner : Lewis, Monica  
Docket No : TI-31794  
Customer No : 23494

**BRIEF ON APPEAL**

Mail Stop Appeal Brief-Patents  
Commissioner for Patents  
PO Box 1450  
Alexandra, VA 22313-1450

Dear Sir:

In support of their appeal of the Final Rejection of claims in this application, and in response to an Office communication dated April 20, 2006, applicants respectfully submit their brief.

### **REAL PARTY IN INTEREST**

The real party in interest is Texas Instruments Incorporated, a Delaware corporation with offices at 7839 Churchill Way, Dallas, Texas 75251.

### **RELATED APPEALS AND INTERFERENCES**

There are no known related appeals or interferences.

### **STATUS OF CLAIMS**

This is an appeal of claims 25 through 31, all of the rejected claims. Claims 1 through 24 and claims 32 through 37 are canceled from consideration.

### **STATUS OF AMENDMENTS**

This appeal is from a non-final action of April 20, 2006. No amendment to the claims under appeal has been filed.

### **SUMMARY OF CLAIMED SUBJECT MATTER**

Claims 25 and 29 are independent claims. Claims 25 describes a device that has the following elements:

- a. an integrated circuit chip having a plurality of contact pads, described on page 11, the first and second paragraph, depicted as element 104 in Figure 1;
- b. a single-layered insulating interposer film having a top surface and a bottom surface, described on page 9, third paragraph, depicted as element 101 in Figure 1;
- c. an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating film, described on page 10, first paragraph, depicted as element 103 in Figure 1;
- d. vias extending through the interposer filled with conductive material, which contact the conductive pattern and form exit ports on the bottom surface, the bottom surface immediately

adjacent the exit ports free of a conductive pattern and contact pad, described in the first and the second paragraph of page 13, depicted as element 107b in Figure 1; and

- e. thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer, described in the first, second, and third paragraph of page 12, and depicted as element 106 in Figure 1.

Claim 29 describes a substrate for connecting an integrated circuit chip.

The substrate has the following elements:

- a. a single-layered insulating interposer film, described on page 9, third paragraph, depicted as element 101 in Figure 1;
- b. an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating interposer film, described on page 10, first paragraph, depicted as element 103 in Figure 1;
- c. vias extending through the interposer, filled with conductive material, contacting the conductive pattern, and forming exit ports on the bottom surface; and the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad, described in the first and the second paragraph of page 13, depicted as element 107b in Figure 1.

#### **GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 25 through 31 are rejected under 35 U.S.C. 103(a) as obvious over Miles et al.<sup>1</sup> in view of Taniguchi et al.<sup>2</sup>

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<sup>1</sup> US Patent No. 5,535,101, issued Jul. 9, 1996, on an application filed Nov. 3, 1992 by Miles et al.

<sup>2</sup> US Patent No. 5,953,592, issued Sep. 14, 1999, on an application filed Jul. 28, 1998 by Taniguchi et al.

## ARGUMENTS

### **Issue I: Whether claim 25 is patentable under 35 U.S.C. 103(a) over Miles et al. in view of Taniguchi et al.**

As stated in a previous section of this paper, claim 25 describes a device that comprises five elements:

- a. an integrated circuit chip having a plurality of contact pads
- b. a single-layered insulating interposer film
- c. an electrically conductive pattern on the top surface of the insulating film
- d. vias filled with conductive material extending through the interposer, forming exit ports;
- e. the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad; and
- f. electrical coupling members disposed between the contact pads and conductive lines.

The Office Action acknowledges that the Miles reference discloses elements (a), (b), (c), (d), and (f); but does not disclose element (e). And argues that the Taniguchi reference cures this defect and it would be obvious to one having ordinary skill to modify the semiconductor device of Miles to include the missing element "because it aids in protecting the device from bulging."<sup>3</sup>

Applicants respectfully submit that the reason to combine the teaching of the Taniguchi reference with the Miles device as suggested in the Office Action is not supported either in the references or in the knowledge of one of ordinary skill in the art, or, from the nature of the problem to be solved.

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<sup>3</sup> Office Action of April 20, 2006, page 3.

First, a close reading of the Taniguchi reference reveals the nature of the bulging device problem and the proposed solution to this problem; and why it is totally irrelevant to the device described in claim 25 of applicants' application.

In the BACKGROUND OF THE INVENTION section of the Taniguchi reference, the source of the bulging device is clearly explained:

In the semiconductor device in which the semiconductor chip is fixed on to the TAB tape by the die bonding material and sealed by the sealing resin, moisture is contained in the polyimide constituting the TAB tape, the sealing resin and the die bonding material. Especially, the polyimide making up the TAB tape is a material which is easily absorbs moisture. Therefore, when the solder balls are reflowed to mount the semiconductor device to the motherboard, the moisture contained in the TAB tape, the sealing resin and the die bonding material is evaporated with the increase in temperature and the vapor causes cracking and/or bulging of the semiconductor device.<sup>4</sup>

It is the evaporating moisture contained in the TAB tape, the sealing resin and the die bonding material during the reflow process that causes the cracking or bulging of the semiconductor device. In the device of claim 25, there is no mentioning of a TAB tape, a sealing resin, or a die bonding material. Therefore, the solution proposed in the Taniguchi reference necessarily does not apply to the device described in claim 26.

Second, the solution proposed by the Taniguchi reference is explained in the SUMMARY OF THE INVENTION section of the reference:

... the method comprising the steps of fixing the semiconductor chip to the tape by the adhesive resin layer, and forming at least one hole in the tape after the step of fixing the semiconductor chip to the tape by the adhesive resin layer.

In this arrangement having at least one hole formed in the tape, the moisture contained in the semiconductor device is released through the at least one hole when the solder balls are reflowed, to thereby prevent cracking and bulging of the semiconductor device. Since the hole is formed after the step of fixing the semiconductor chip to the tape by the adhesive resin layer, the hole is not filled up with the adhesive resin layer which may flow at the time of heat treatment

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<sup>4</sup> Taniguchi, *supra*, col. 1, lines 47 through 58.

during the semiconductor fabrication process and thus effectively functions as a vapor escape hole.<sup>5</sup>

The solution proposed by the Taniguchi reference for solving the evaporation moisture problem is to form one hole in the tape after the step of fixing the chip to the tape so that it is not filled up with adhesive resin and therefore can function as a vapor escape hole. A hole not filled with adhesive resin is not an element in the device described in claim 25 of applicants' application because claim 25 does not disclose a device that employs adhesive resin.

Applicants respectfully submit that the motivation to combine as suggested in the Office Action is misplaced because the combination would be to solve a non-problem in the device described in claim 25. And for a person of ordinary skill in the art, this fact would be obvious – the nature of the problem to be solved does not concern the device described in claim 25.

For the reason stated above, applicants respectfully submit that because the Office Action fails to support a motivation to combine the references, it fails to establish a *prima facie* case of obviousness against claim 25 based on the cited references.

**Issue II: Whether claim 28 is patentable under 35 U.S.C. 103(a) over Miles et al. in view of Taniguchi et al.**

Claim 28 describes a substrate for connecting an integrated circuit chip. The substrate has the following elements:

- a. a single-layered insulating interposer film;
- b. an electrically conductive pattern on the top surface of the insulating interposer film;
- c. vias extending through the interposer, filled with conductive material forming exit ports on the bottom surface; and

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<sup>5</sup> *Id.* col. 2, lines 26 through 40.

- d. the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad.

The Office Action rejects claim 28 on exactly the same ground as regarding claim 25 – the Miles reference fails to disclose element (d) but the Taniguchi reference cures the defect and the motivation for combining the teaching of the two references is that “it aids in protecting the device from bulging.”<sup>6</sup>

Clearly, the causes of the problem that the Taniguchi reference is purported to solve is absent in the substrate described in claim 28 of applicants’ application. There is no mentioning of a TAB tape, no mentioning of an adhesive resin and no mentioning of a die bonding material, where moisture may be absorbed.

For this same reason, applicants respectfully submit that the motivation to combine the two references is misplaced because the combination would be to solve a non-problem in the device described in claim 28. And for a person of ordinary skill in the art, this fact would be obvious – the nature of the problem to be solved does not concerns the device described in claim 28. Therefore, applicants respectfully submit that because the Office Action fails to support a motivation to combine the references, it fails to establish a *prima facie* case of obviousness against claim 28 based on the cited references.

**Issue III: Whether claims 26, 27, 29, 30, and 31 are patentable under 35 U.S.C. 103(a) over Miles et al. in view of Taniguchi et al.**

Claims 26 and 27 properly depend from claim 25 and claims 29 through 31 properly depend from claim 28. Because the Office Action fails to establish a *prima facie* case of obviousness against claims 25 and 28, applicants respectfully submit that the references do not render the dependent claims of claims 25 and 28.

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<sup>6</sup> Office Action, *supra*, page 4.

**Conclusion**

The motivation suggested in the Office Action to combine the cited references is not supported by the reference, or in the knowledge of a person of ordinary skill in the art, or in the nature of the problem to be solved. Therefore, the Office action fails to establish a *prima facie* case of obviousness against the independent claims 25 and 28 and their dependent claims.

Applicants respectfully request the Board to reverse the final rejection and allow the claims on appeal.

Respectfully submitted,  
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## **CLAIMS APPENDIX**

The claims on appeal read as follows. Claims 1 through 24 and claims 32 through 37 have been canceled from examination.

### **In the Claims:**

1-24. (canceled)

25.       A device comprising:

an integrated circuit chip having a plurality of contact pads;

a single-layered insulating film having a top surface and a bottom surface;

an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating film;

vias extending through the interposer filled with conductive material, contacting the conductive pattern, and forming exit ports on the bottom surface;

the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad; and

thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer.

26.       The device of claim 25, further comprising solder balls attached to the exit ports.

27.       The device of claim 25, further comprising encapsulating material encapsulating the integrated circuit chip.

28.       A substrate for connecting an integrated circuit chip having a plurality of contact pads, comprising:

a single-layered insulating interposer film having a top surface and a bottom surface;

an electrically conductive pattern formed of a conductive film disposed on the top surface of the insulating interposer film;

vias extending through the interposer, filled with conductive material, contacting the conductive pattern, and forming exit ports on the bottom surface; and

the bottom surface immediately adjacent the exit ports free of a conductive pattern and contact pad.

29. The substrate in claim 28, further comprising solder balls attached to the exit ports.

30. The substrate in claim 28, in which the conductive pattern includes attachment sites corresponding to contact pads on the integrated circuit chip.

31. A device comprising a substrate in claim 28, and an integrated chip attached to the substrate.

32-37. (canceled)

**EVIDENCE APPENDIX**

None

**RELATED PROCEEDINGS APPENDIX**

None